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09/973,058	10/10/2001	Toshio Sakurai	35.C15866	5036

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EXAMINER	
MILIA, MARK R	

ART UNIT	PAPER NUMBER
2625	

DATE MAILED: 03/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/973,058	SAKURAI, TOSHIO	
	Examiner	Art Unit	
	Mark R. Milia	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 December 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 November 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Applicant's amendments were received on 11/3/05 and 12/30/05 and have been entered and made of record. Currently, claims 1-16 are pending.

Drawings

2. Applicant's amendment to Figure 7 to label the figure as prior art has overcome the objection as cited in the previous Office Action. Therefore the objection has been withdrawn.

Claim Rejections - 35 USC § 112

3. Applicant's amendment to claims 1, 2, 5-7, and 10 has overcome the rejection of claims 1-10 as being indefinite. Therefore the rejection of claims 1-10 has been withdrawn.

Response to Arguments

4. Applicant's arguments with respect to claims 1-16 have been considered but are moot in view of the current amendment to the claims and therefore a new ground(s) of rejection will be made. Newly added claims 11-16 will be addressed in the following rejection.

Claim Rejections - 35 USC § 102

5. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

6. Claims 15 and 16 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5831683 to Matsumoto et al.

Regarding claim 15, Matsumoto discloses an interface apparatus for inputting information from an external apparatus, comprising: a timer for timing a predetermined time (see Fig. 1 and column 4 lines 22-39) and a comparator for making a comparison between a length of a low level state in input information within the predetermined time timed by said timer, and a length of a high level state in the input information within the predetermined time, and for outputting a low level signal if the comparison shows that the length of the low level state is longer than the length of the high level state, and outputting a high level signal if the comparison shows that the length of the high level

state is longer than the length of the low level state (see Figs. 1, 4, and 5 and column 5 line 23-column 6 line 23).

Regarding claim 16, Matsumoto further discloses wherein said timer outputs a trigger after an elapse of the predetermined time from a delimiter existing in the input information, and said comparator inputs the trigger and makes the comparison in accordance with the trigger (see Fig. 1, column 4 lines 22-39, and column 4 line 62-column 6 line 23).

Claim Rejections - 35 USC § 103

7. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

8. Claims 1, 2, 4, 6, 7, and 11-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wakasugi in view of U.S. Patent No. 6453272 to Slechta.

Regarding claims 1 and 6, Wakasugi discloses an interface apparatus and information processing method for inputting information from an external apparatus, comprising: a first circuit for, in a case where there is a change in information input from the external apparatus, fetching the information after an elapse of a predetermined time (see Figs. 10-12 and column 11 lines 17-47) and a second circuit for invalidating a sequence of data that is detected as being noise by the change in the input signal over a certain period of time (see column 12 lines 14-27 and column 12 line 42-column 13 line 4).

Wakasugi does not disclose expressly a second circuit for, determining whether the information fetched by the first circuit matches a protocol of the information input from the external apparatus, and when the information fetched by said first circuit is not matched with the protocol of the information input from the external apparatus, skipping the fetched information according to the protocol.

Slechta discloses a circuit for, determining whether the information fetched by the first circuit matches a protocol of the information input from the external apparatus, and when the information fetched by said first circuit is not matched with the protocol of the information input from the external apparatus, skipping the fetched information according to the protocol (see Fig. 3, column 1 lines 50-52, and column 5 line 62-column 6 line 16, reference shows that when a signal exceeds a predetermined noise threshold a noise filtering process is performed, otherwise the signal is passed unchanged, analogous to the skipping of information that does not match a protocol).

Regarding claim 13, Wakasugi discloses a data change detector for detecting a change in information input from the external apparatus and outputting a reset upon the detection of the change (see Fig. 10 (10) and column 3 line 65-column 4 line 10), a timer for inputting the reset output by said change detector and outputting a trigger after the elapse of a predetermined time from the input of the reset (see Fig. 12 and column 12 lines 14-65), a data latch for inputting the trigger output by said timer and fetching information upon the input of the trigger (see Fig. 10, column 9 lines 40-63, and column 10 line 61-column 11 line 16), and a circuit for invalidating a sequence of data that is

detected as being noise by the change in the input signal over a certain period of time (see column 12 lines 14-27 and column 12 line 42-column 13 line 4).

Wakasugi does not disclose expressly a logical filter for, determining whether the information fetched by the first circuit matches a protocol of the information input from the external apparatus, and when the information fetched by said first circuit is not matched with the protocol of the information input from the external apparatus, skipping the fetched information according to the protocol.

Slechta discloses a logical filter for, determining whether the information fetched by the first circuit matches a protocol of the information input from the external apparatus, and when the information fetched by said first circuit is not matched with the protocol of the information input from the external apparatus, skipping the fetched information according to the protocol (see Fig. 3, column 1 lines 50-52, and column 5 line 62-column 6 line 16, reference shows that when a signal exceeds a predetermined noise threshold a noise filtering process is performed, otherwise the signal is passed unchanged, analogous to the skipping of information that does not match a protocol).

Regarding claim 14, Wakasugi discloses a data change detector for detecting a change in information input from the external apparatus and outputting a reset upon the detection of the change (see Fig. 10 (10) and column 3 line 65-column 4 line 10), a timer for inputting the reset output by said change detector and outputting a trigger after the elapse of a predetermined time from the input of the reset (see Fig. 12 and column 12 lines 14-65), a data latch for inputting the trigger output by said timer and fetching information upon the input of the trigger (see Fig. 10, column 9 lines 40-63, and column

10 line 61-column 11 line 16), and a logical filter for invalidating a sequence of data that is detected as being noise by the change in the input signal over a certain period of time (see column 12 lines 14-27 and column 12 line 42-column 13 line 4).

Wakasugi does not disclose expressly determining whether the information fetched by the latch matches a protocol of the information input from the external apparatus, and when the information fetched by said latch is matched with the protocol information input from the external apparatus, outputting the fetched information.

Slechta discloses determining whether the information fetched by the latch matches a protocol of the information input from the external apparatus, and when the information fetched by said latch is matched with the protocol information input from the external apparatus, outputting the fetched information (see Fig. 3, column 1 lines 50-52, and column 5 line 62-column 6 line 16, reference shows that when a signal exceeds a predetermined noise threshold a noise filtering process is performed, otherwise the signal is passed unchanged, analogous to outputting the signal).

Wakasugi & Slechta are combinable because they are from the same field of endeavor, the elimination of noise is transmission signals.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine the matching of a protocol as criteria to skip or alter data, as described by Slechta, with the system of Wakasugi.

The suggestion/motivation for doing so would have been to accurately suppress spurious noise, such as input glitches, without introducing artifacts of conventional low-pass filters (see column 1 lines 42-44 of Slechta).

Therefore, it would have been obvious to combine Slechta with Wakasugi to obtain the invention as specified in claims 1, 6, and 13.

Regarding claims 2 and 7, Wakasugi and Slechta disclose the system discussed in claims 1 and 6, and Wakasugi further discloses a data change detector for outputting a reset in the case where there is a change in the information input from the external apparatus (see Fig. 10 (10) and column 3 line 65-column 4 line 10), a timer for inputting the reset output by the change detector and outputting a trigger after the elapse of a predetermined time from the input of the reset (see Fig. 12 and column 12 lines 14-65), a data latch for inputting the trigger output by said timer and fetching the information (see Fig. 10, column 9 lines 40-63, and column 10 line 61-column 11 line 16).

Regarding claim 4, Wakasugi and Slechta disclose the system discussed in claim 1, and Wakasugi further discloses wherein the information which is inputted from the external apparatus is inputted to the first circuit and the information fetched by said first circuit is input to the second circuit (see Fig. 10 and column 11 line 17-column 12 line 65).

Regarding claims 11 and 12, Wakasugi and Slechta disclose the system discussed in claims 1 and 6, and Slechta further discloses wherein, if the fetched information continuously repeats a same value, said second circuit skips the fetched information (see Fig. 3, column 1 lines 50-52, and column 5 line 62-column 6 line 16, reference shows that when a signal exceeds a predetermined noise threshold a noise

filtering process is performed, otherwise the signal is passed unchanged, analogous to the skipping of information that is being repeated).

9. Claims 5 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wakasugi and Slechta in view of Sotokawa.

Regarding claims 5 and 10, Wakasugi discloses a first circuit for, when the inputted information is information which was changed within a predetermined time, invalidating said information (see Figs. 10-12 and column 11 lines 17-47) and a second circuit for invalidating a sequence of data that is detected as being noise by the change in the input signal over a certain period of time (see column 12 lines 14-27 and column 12 line 42-column 13 line 4).

Wakasugi does not disclose expressly a second circuit for, determining whether the information fetched by the first circuit matches a protocol of the information input from the external apparatus, and when the information fetched by said first circuit is not matched with the protocol of the information input from the external apparatus, skipping the fetched information according to the protocol and a printer engine for printing the information fetched by the first circuit, if it is determined by the second circuit that the information fetched by the first circuit matches the protocol of the information input from the external apparatus.

Slechta discloses a circuit for, determining whether the information fetched by the first circuit matches a protocol of the information input from the external apparatus, and when the information fetched by said first circuit is not matched with the protocol of the

information input from the external apparatus, skipping the fetched information according to the protocol (see Fig. 3, column 1 lines 50-52, and column 5 line 62-column 6 line 16, reference shows that when a signal exceeds a predetermined noise threshold a noise filtering process is performed, otherwise the signal is passed unchanged, analogous to the skipping of information that does not match a protocol).

Sotokawa discloses a printer engine for printing the information fetched by the first circuit, if it is determined by the second circuit that the information fetched by the first circuit matches the protocol of the information input from the external apparatus (see Figs. 4 and 5, column 6 lines 29-36 and 58-62, column 8 lines 22-27, and column 10 line 55-column 11 line 2).

Wakasugi, Slechta, & Sotokawa are combinable because they are from the same field of endeavor, detection and processing of changes in transmitted information.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine the printer as an external device as described by Sotokawa with the system of Wakasugi and Slechta.

The suggestion/motivation for doing so would have been to allow the desired information to be printed, as it is well known in the art to provide a printer as an external device to output data information.

Therefore, it would have been obvious to combine Sotokawa with Wakasugi and Slechta to obtain the invention as specified in claims 5 and 10.

10. Claims 3 and 8 rejected under 35 U.S.C. 103(a) as being unpatentable over Wakasugi and Slechta as applied to claims 1 and 6 above, and further in view of Sotokawa.

Wakasugi and Slechta do not disclose expressly wherein said external apparatus forms the information such that same information does not continue.

Sotokawa discloses wherein said external apparatus forms the information such that same information does not continue (see Figs. 4 and 5, column 6 lines 29-36 and 58-62, column 8 lines 22-27, and column 10 line 55-column 11 line 2).

Wakasugi, Slechta, & Sotokawa are combinable because they are from the same field of endeavor, detection and processing of changes in transmitted information.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine the printer as an external device as described by Sotokawa with the system of Wakasugi and Slechta.

The suggestion/motivation for doing so would have been to allow the desired information to be printed, as it is well known in the art to provide a printer as an external device to output data information.

Therefore, it would have been obvious to combine Sotokawa with Wakasugi and Slechta to obtain the invention as specified in claims 3 and 8.

11. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wakasugi and Slechta as applied to claim 6 above, and further in view of Chapman.

Wakasugi discloses the use of logic and logic filters in the execution of the invention (see column 11 line 17-column 12 line 65).

Wakasugi and Slechta do not disclose expressly wherein the first step is executed by a glitch noise filter.

Chapman discloses the use of glitch noise filters to filter data information (see column 1 lines 36-59 and column 7 lines 44-53).

Wakasugi, Slechta, & Chapman are combinable because they are from the same field of endeavor, detection and processing of changes in transmitted information.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine the use of a glitch noise filter as described by Chapman with the system of Wakasugi and Slechta.

The suggestion/motivation for doing so would have been to accurately filter noise signals from incoming information.

Therefore, it would have been obvious to combine Chapman with Wakasugi and Slechta to obtain the invention as specified in claim 9.

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. To further show the state of the art refer to the attached Notice of references Cited.

13. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mark R. Milia whose telephone number is (571) 272-7408. The examiner can normally be reached M-F 8:00am-4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Twyler M. Lamb can be reached at (571) 272-7406. The fax number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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